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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/789,637	02/27/2004	Brian S. Schieck	NVID-P001125	7655

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EXAMINER	
DUONG, KHANH B	

ART UNIT	PAPER NUMBER
2822	

MAIL DATE	DELIVERY MODE
10/05/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/789,637	SCHIECK ET AL.	
	Examiner	Art Unit	
	Khanh B. Duong	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 July 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) *8-12 and 19-35* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 13-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on July 16, 2007 has been entered.

Response to Amendment

This office action is in response to the amendment filed on July 16, 2007.

Accordingly, claims 1 and 13 were amended.

Claims 8-12 and 19-35 remain withdrawn from further consideration as being drawn to a nonelected inventions, there being no allowable generic or linking claim.

Currently, claims 1-7 and 13-18 remain active.

Response to Arguments

Applicant's arguments with respect to the amended claims have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim 1 and 3-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheng et al. (U.S. 6,686,615) in view of Potts (U.S. 2003/0124816 A1).

Cheng et al. ("Cheng") discloses in FIGs. 2-4 a semiconductor die 10 comprising: a conductive test signal bump 40 for transmitting test signals off of said semiconductor die 10; a test signal redistribution layer trace 21 for communicating said test signals to said conductive test signal bump 40, wherein said test signal redistribution layer trace 21 is included in a redistribution layer (14, 21 & 30) and said test signal redistribution trace 21 is disposed such that multiple test signals (from multiple testing pads 23, see

FIG. 2) are accessible at varying degrees of electronic component granularity, said test signal redistribution layer trace 21 communicatively coupled to said conductive test signal bump 40; and a test probe point 23 for accessing said test signals in said semiconductor die 10 and for electrical coupling to said redistribution layer.

Re claim 1, Cheng does not disclose the multiple test signals are accessible at varying degrees of electronic component granularity along said test signal redistribution layer trace.

Potts expressly shows in FIGs. 3 and 4 multiple test signals (from various transistors 42a & 42b) are accessible (via a shared pad SP_x) at varying degrees of electronic component granularity (e.g. various transistors 42a & 42b) along a test signal redistribution layer trace 62. Potts states that the use of a shared pad SP_x minimizes the number of test probe tips required to access the contact pads associated with the various transistors on a semiconductor die during testing [see page 4, paragraph 0029].

Since Cheng and Potts are from the same field of endeavor, the purpose disclosed by Potts would have been recognized in the pertinent prior art of Cheng.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the device disclosed by Cheng as suggested by Potts because of the desirability to minimize the number of test probe tips required to access the contact pads associated with the various transistors on a semiconductor die during testing, thus reducing operating costs.

Re claims 3-5, the claims recite the following product-by-process limitations: "accessible by drilling" (claim 3); "a focused ion beam (FIB) pad accessible by focused

ion beam drilling and conductive material backfill" (claim 4); and "conductive material backfill" (claim 5). However, these limitations have not been given patentable weight because product-by-process claims are not limited to the manipulations of the recited steps, only the structure implied by the steps. "[E]ven though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985). Thus, Cheng discloses in FIG. 3 the test probe point 23 comprises a bonding pad which is coupled to said test signal redistribution layer (14, 21 and 30).

Re claim 6, Cheng expressly shows in FIG. 2 said test signal redistribution layer trace 21 is routed in a spiral (winding) pattern.

Claim 13, 14 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin (U.S. 5,258,648) in view of Potts (U.S. 2003/0124816 A1).

Lin discloses a semiconductor device in FIGs. 1-5 comprising: a package substrate 22 for communicating test signals on an external access point 28; wherein said package substrate 22 includes a conductive trace 26 disposed such that multiple test signals (from multiple testing pads 27, see FIG. 1) are accessible at varying degrees of electronic component granularity; and a semiconductor die 12 having test

probe points 16 accessible by said external access point 28, wherein said semiconductor die 12 is electrically coupled to said package substrate 22.

Re claim 13, Lin does not disclose the multiple test signals are accessible at varying degrees of electronic component granularity along said conductive trace.

Potts expressly shows in FIGs. 3 and 4 multiple test signals (from various transistors 42a & 42b) are accessible (via a shared pad SP_x) at varying degrees of electronic component granularity (e.g. various transistors 42a & 42b) along a conductive trace 62. Potts states that the use of a shared pad SP_x minimizes the number of test probe tips required to access the contact pads associated with the various transistors on a semiconductor die during testing [see page 4, paragraph 0029].

Since Lin and Potts are from the same field of endeavor, the purpose disclosed by Potts would have been recognized in the pertinent prior art of Lin.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the device disclosed by Lin as suggested by Potts because of the desirability to minimize the number of test probe tips required to access the contact pads associated with the various transistors on a semiconductor die during testing, thus reducing operating costs.

Re claim 14, Lin expressly discloses in FIG. 5 said package substrate 22 comprises: a first surface with ball grid array 32; a second surface with conductive contacts 26 for electrically coupling with conductive bumps 16 of said semiconductor die 12; and a trace for electrically coupling one of said conductive contacts 26 to said external access point 28 [see also col. 7, lines 10-27].

Re claim 18, Lin discloses said external access point 28 is accessible by automatic test equipment [see col. 7, lines 25-27].

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cheng and Potts as applied to claims 1 and 3-7 above, and further in view of Lin.

Re claim 2, Cheng expressly discloses in FIG. 3 that said semiconductor die 10 is a flip chip die configured for connection to an inherent package substrate. However, Cheng fails to specifically mention the conductive bump 40 being electrically coupled to a test signal access component of a package substrate. Potts also does not disclose the same.

Lin shows in FIG. 5 to electrically couple the conductive bumps 16 of a semiconductor die 12 to a test signal access component 28 of a package substrate 22 [see col. 7, lines 10-27].

Since Cheng, Potts and Lin are from the same field of endeavor, the purpose disclosed by Lin would have been recognized in the pertinent prior art of Cheng and Potts.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the combined device disclosed by Cheng and Potts as taught by Lin, since Lin states at column 7, lines 27-31 that such modification would allow the composite flip chip semiconductor device to be tested and burned-in in a known test socket which is capable of handling edge contacts.

Claim 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin and Potts as applied to claims 13, 14 and 18 above, and further in view of Cheng.

Re claims 15 and 17, Lin does not disclose said semiconductor die comprises: a test signal redistribution layer comprising conductive traces; a test probe point for accessing signals in said semiconductor die and for electrical coupling to said test signal redistribution layer; a test access via for electrically coupling said test probe point to said test signal redistribution layer; and a conductive bump for conveying a test signal off of said semiconductor die to said package substrate, said conductive bump located on a first surface of said semiconductor die and electrically coupled to said test signal redistribution layer. On the other hand, Potts expressly shows in FIG. 4 a semiconductor die comprises: a test signal redistribution layer comprising conductive traces (58 and 62); a test probe point (between SP_x and 62) for accessing signals in said semiconductor die and for electrical coupling to said test signal redistribution layer; a test access via SP_x for electrically coupling said test probe point to said test signal redistribution layer.

Re claims 15 and 17, Lin and Potts do not disclose a conductive bump for conveying a test signal off of said semiconductor die to said package substrate, said conductive bump located on a first surface of said semiconductor die and electrically coupled to said test signal redistribution layer routing of said test signal redistribution layer conductive traces is such that trace widths and spacing is a minimum without causing signal interference.

Cheng shows in FIGs. 2 and 3 a semiconductor die 10 comprises: a conductive bump 40 for conveying a test signal off of said semiconductor die 10 inherently to a package substrate, said conductive bump 40 located on a first surface of said semiconductor die 10 and electrically coupled to said test signal redistribution layer [see col. 2, line 41 to col. 3, line 40]. Cheng further appears to expressly disclose in FIG. 2 said test signal redistribution layer conductive traces 21 are routed such that trace widths and spacing is a minimum without causing signal interference.

Since Lin, Potts and Cheng are from the same field of endeavor, the purpose disclosed by Cheng would have been recognized in the pertinent prior art of Lin and Potts.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the combined device disclosed by Lin and Potts as suggested by Cheng , since Cheng states at column 1, lines 55 to 58 that such modification would form redistribution traces having equal lengths to acquire simple circuit design to reduce signal skew.

Re claim 16, the claim recites the following product-by-process limitations: "a focused ion beam (FIB) pad accessible by focused ion beam drilling and conductive material backfill". However, these limitations have not been given patentable weight because product-by-process claims are not limited to the manipulations of the recited steps, only the structure implied by the steps. "[E]ven though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of

production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh B. Duong whose telephone number is (571) 272-1836. The examiner can normally be reached on Monday to Friday from 8:00-4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith, can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KBD

Zandra V. Smith
Supervisory Patent Examiner
1 Oct. 2007